FIG.1

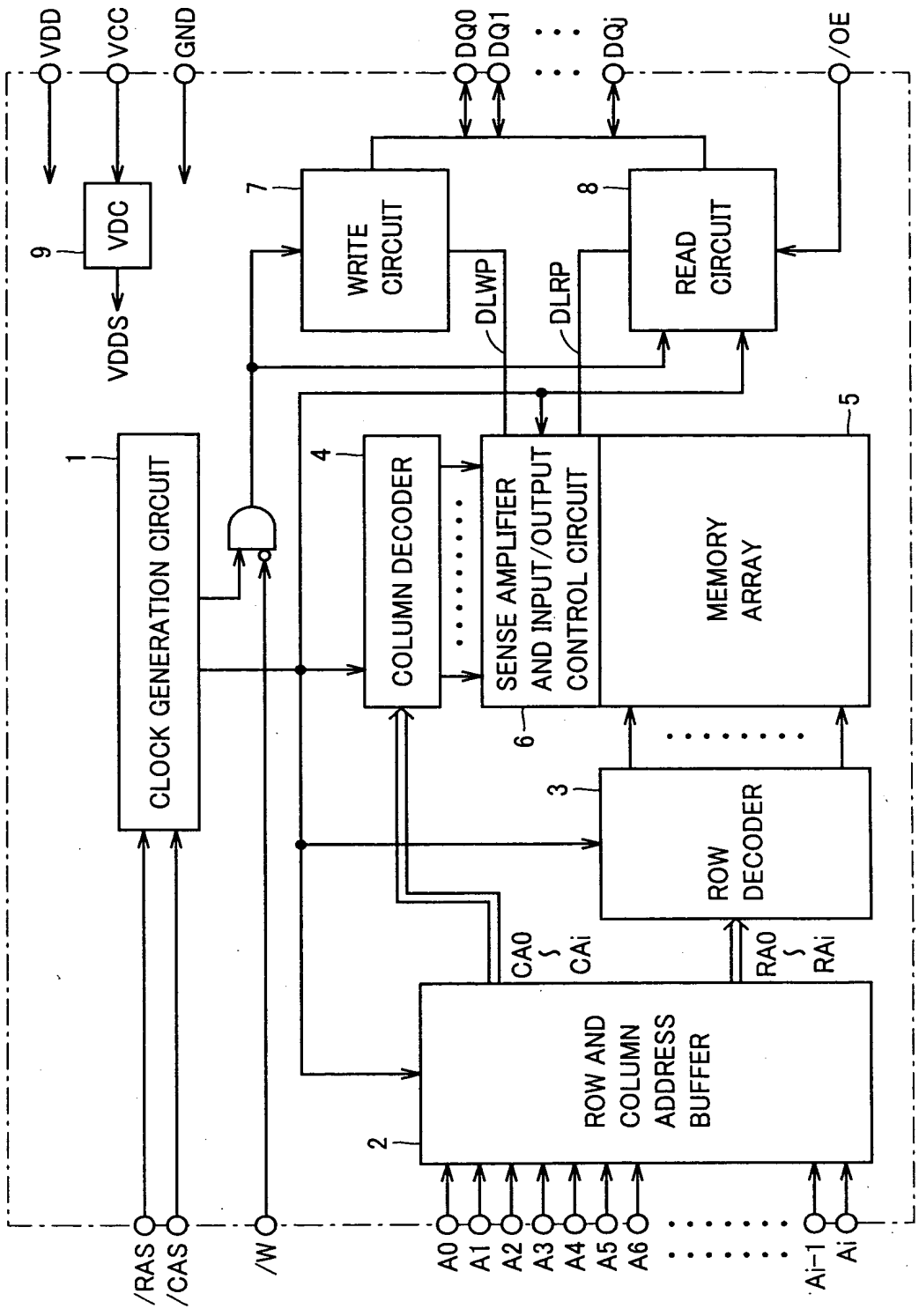

VDD
VCC
GND
DQ0
DQ1
DQj
/OE
9
VDC
VDDS
7
WRITE CIRCUIT
8
READ CIRCUIT
DLWP
DLRP
1
CLOCK GENERATION CIRCUIT
4
COLUMN DECODER
SENSE AMPLIFIER AND INPUT/OUTPUT CONTROL CIRCUIT
6
5
MEMORY ARRAY
3
ROW DECODER
CA0 ~ CAi
RA0 ~ RAi
2
ROW AND COLUMN ADDRESS BUFFER
/RAS
/CAS
/W
A0
A1
A2
A3
A4
A5
A6
Ai-1
Ai

FIG.2

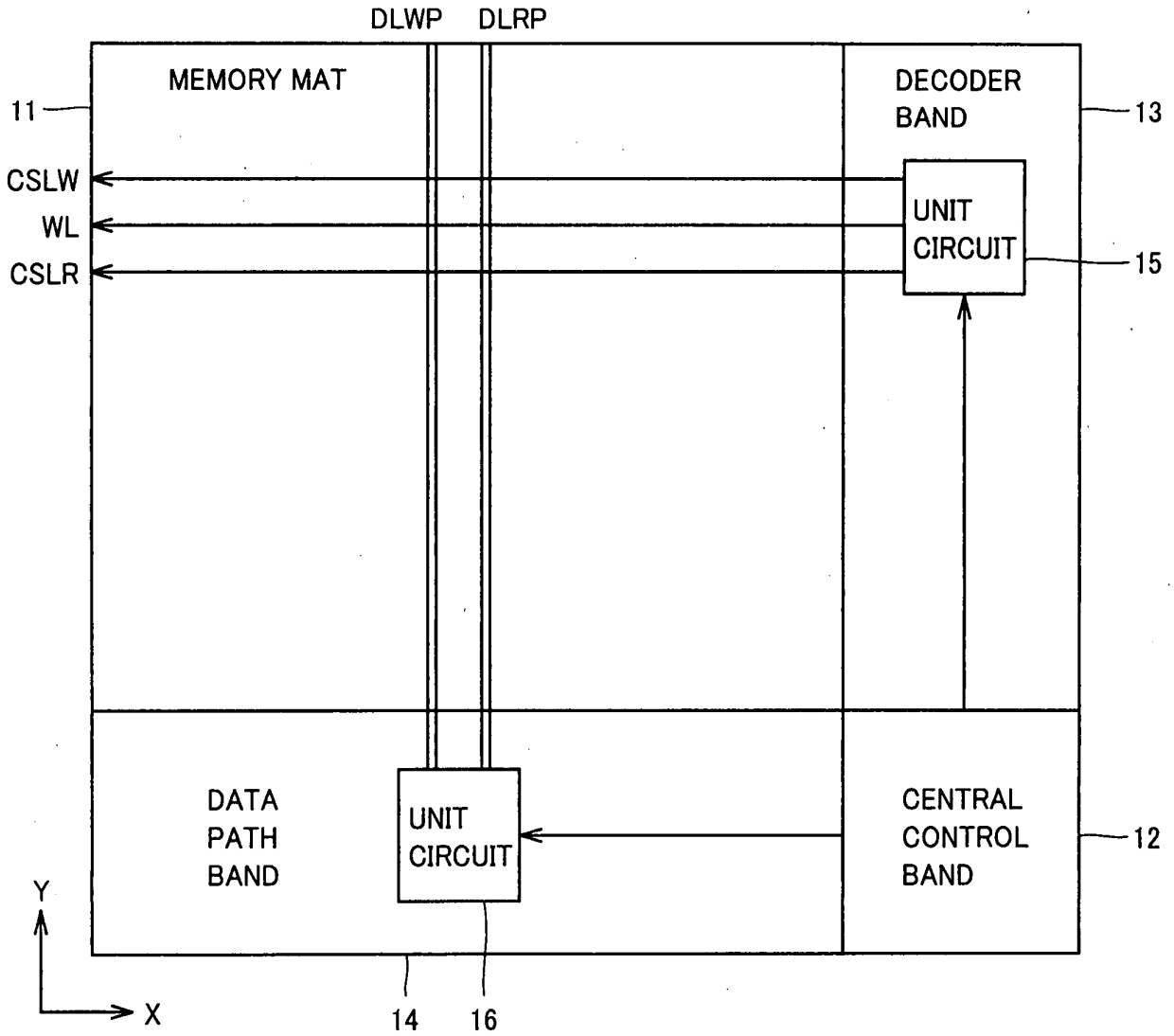

DLWP
DLRP
MEMORY MAT
11
DECODER BAND
13
CSLW
WL
CSLR
UNIT CIRCUIT
15
DATA PATH BAND
UNIT CIRCUIT
CENTRAL CONTROL BAND
12
Y
X
14
16

FIG.3

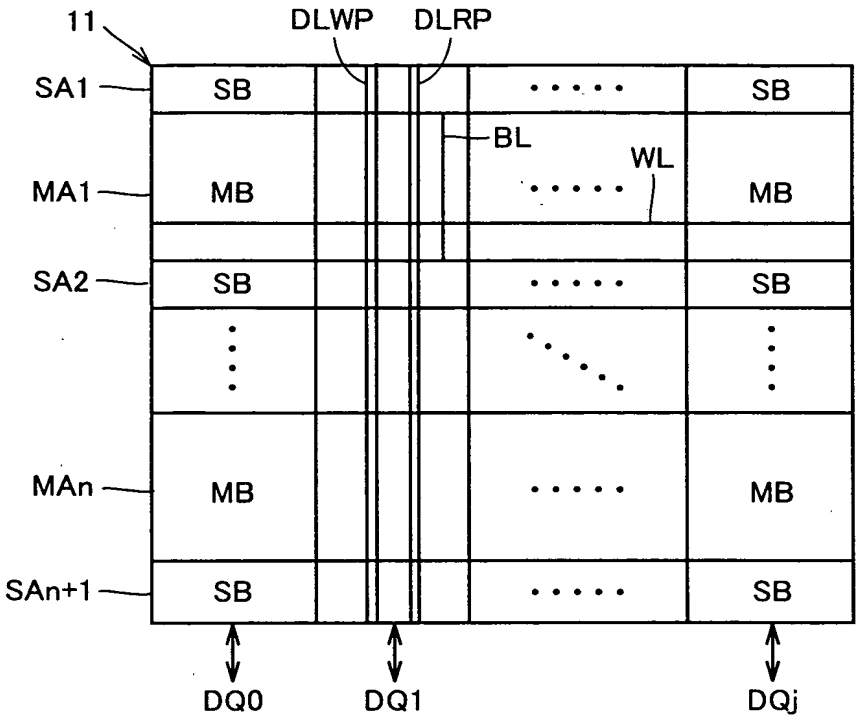

11
DLWP
DLRP
SA1
SB
SB
BL
WL
MA1
MB
MB
SA2
SB
SB
MAn
MB
MB
SAn+1
SB
SB
DQ0
DQ1
DQj

FIG.4

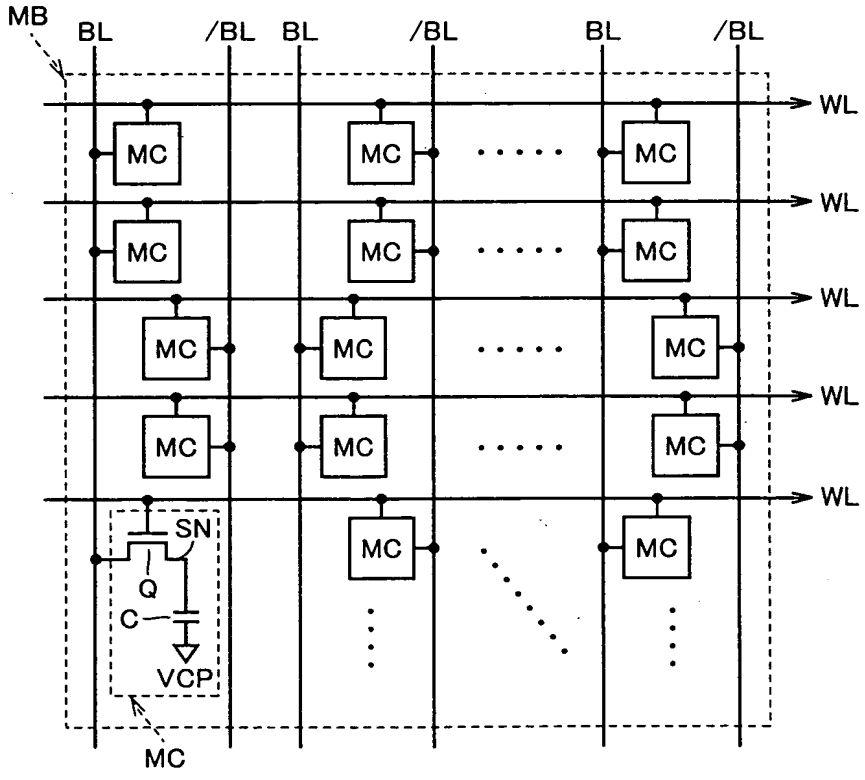

MB
BL
/BL
BL
/BL
BL
/BL
WL
MC
SN
Q
C
VCP
MC

FIG.5

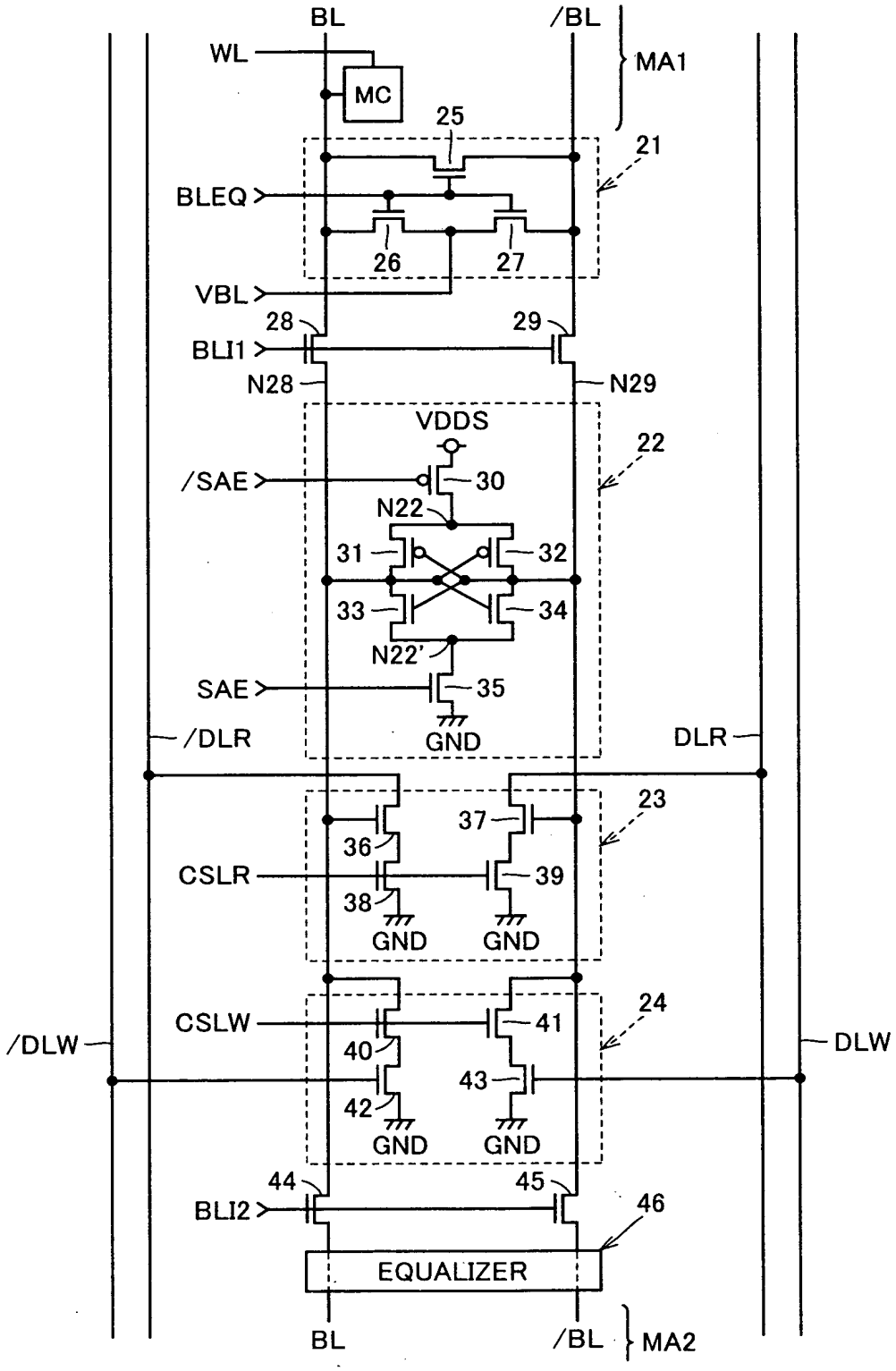

BL
/BL
WL
MC
MA1
25
21
BLEQ
26
27
VBL
28
29
BLI1
N28
N29
VDDS
22
/SAE
30
N22
31
32
33
34
N22'
SAE
35
GND
/DLR
DLR
23
37
36
CSLR
39
38
GND
GND
24
CSLW
41
40
43
42
GND
GND
/DLW
DLW
44
45
BLI2
46
EQUALIZER
BL
/BL
MA2

FIG.6

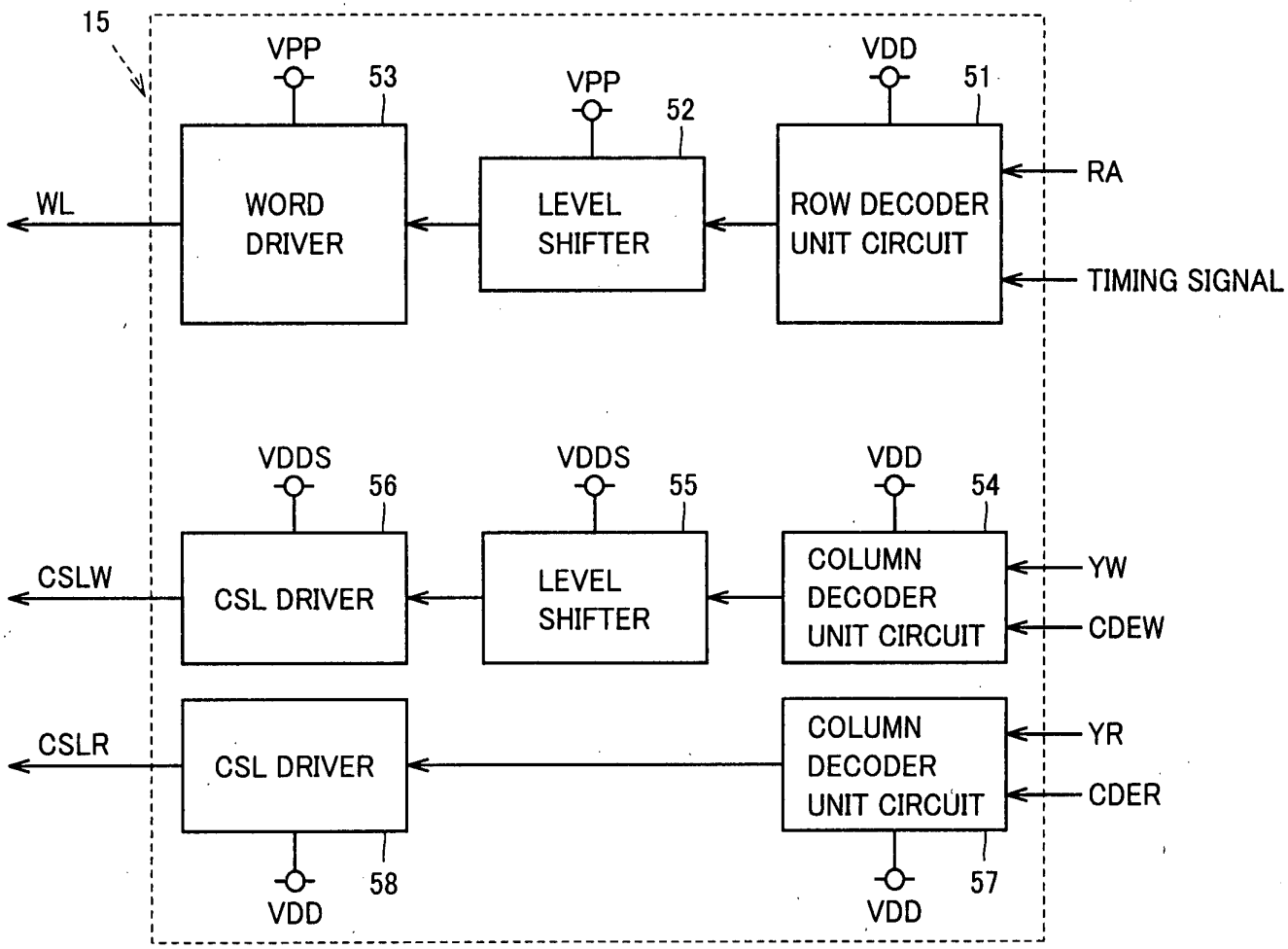

15
VPP
53
VPP
52
VDD
51
WL
WORD DRIVER
LEVEL SHIFTER
ROW DECODER UNIT CIRCUIT
RA
TIMING SIGNAL
VDDS
56
VDDS
55
VDD
54
CSLW
CSL DRIVER
LEVEL SHIFTER
COLUMN DECODER UNIT CIRCUIT
YW
CDEW
CSLR
CSL DRIVER
COLUMN DECODER UNIT CIRCUIT
YR
CDER
VDD
58
VDD
57

FIG.7

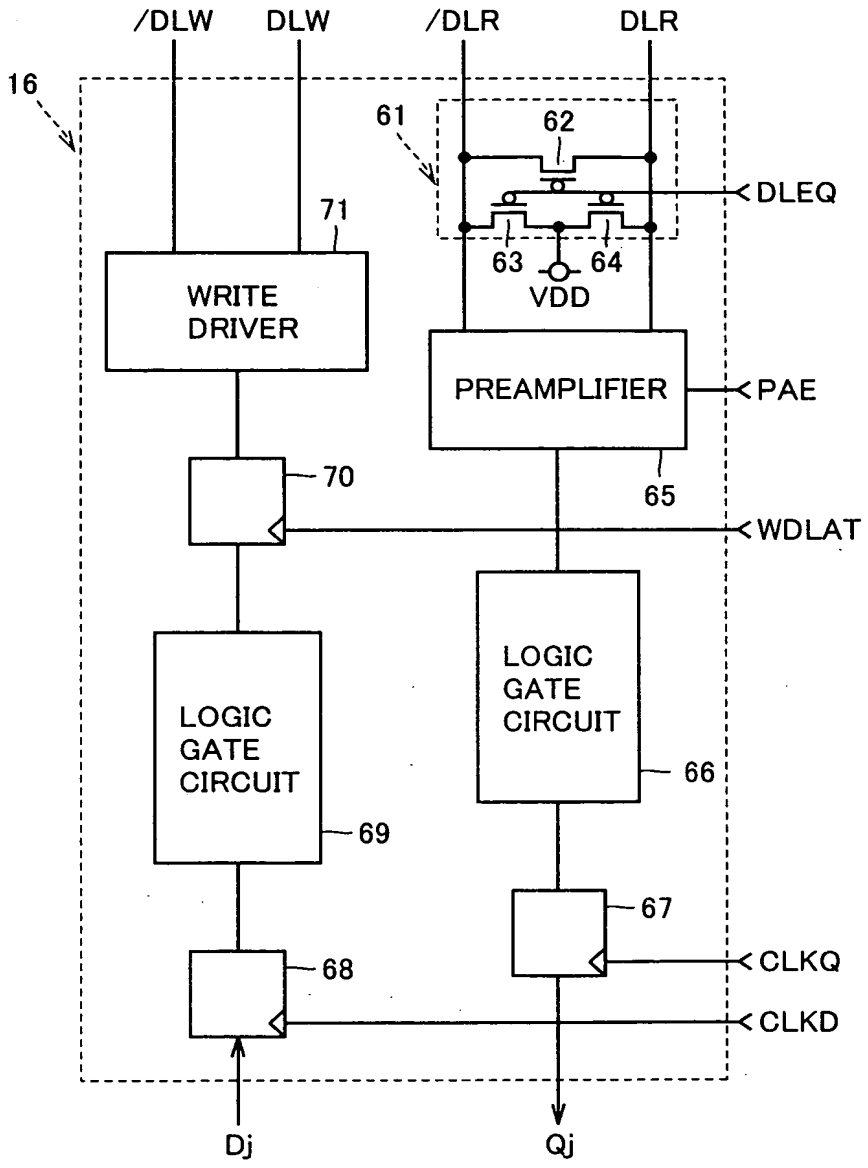

/DLW
DLW
/DLR
DLR
16
61
62
DLEQ
71
63
64
VDD
WRITE DRIVER
PREAMPLIFIER
PAE
70
65
WDLAT
LOGIC GATE CIRCUIT
LOGIC GATE CIRCUIT
66
69
67
68
CLKQ
CLKD
Dj
Qj

FIG.8

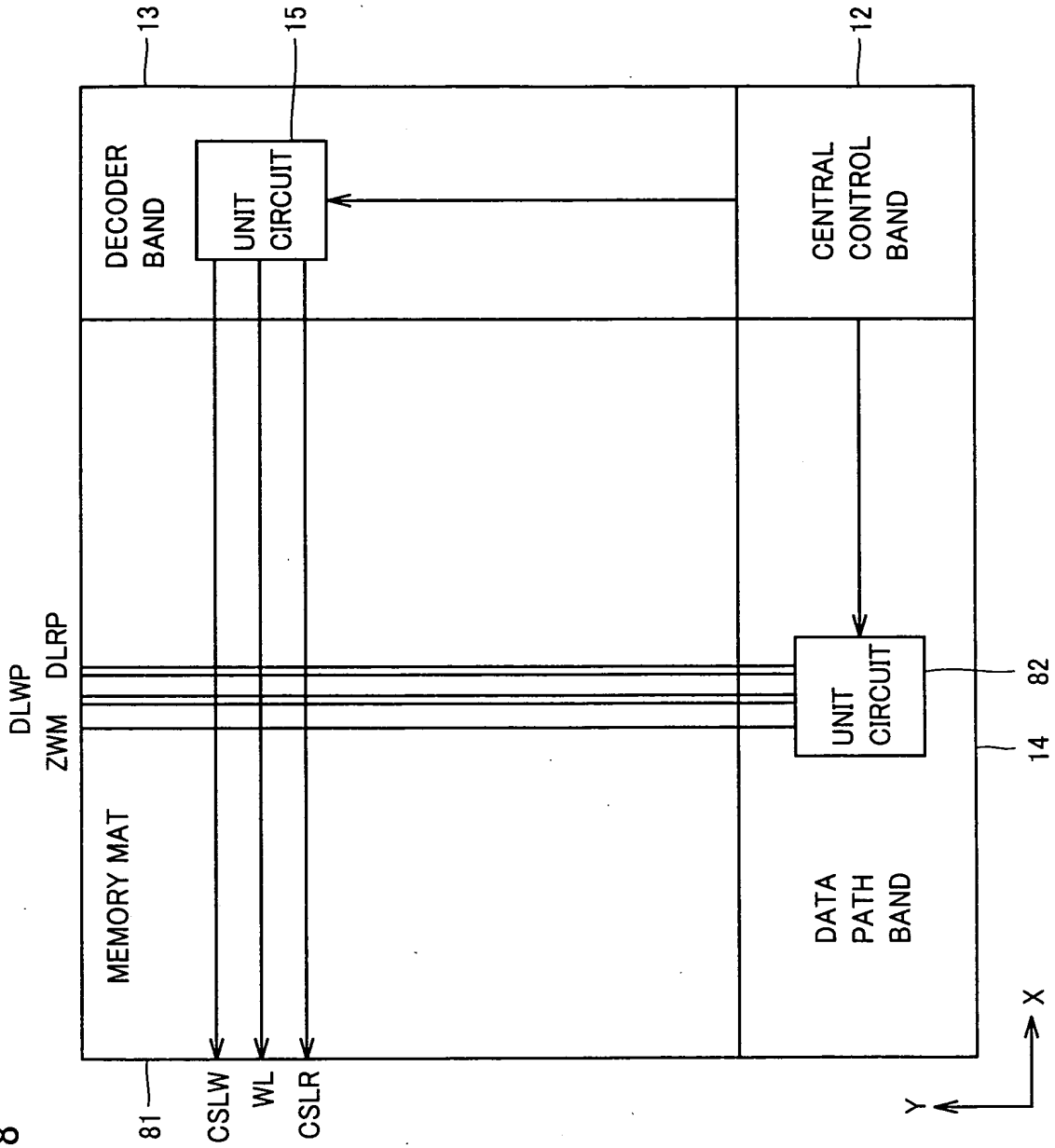

13
15
12
DECODER BAND
UNIT CIRCUIT
CENTRAL CONTROL BAND
DLWP
DLRP
ZWM
UNIT CIRCUIT
82
14
MEMORY MAT
DATA PATH BAND
81
CSLW
WL
CSLR
X
Y

FIG.9

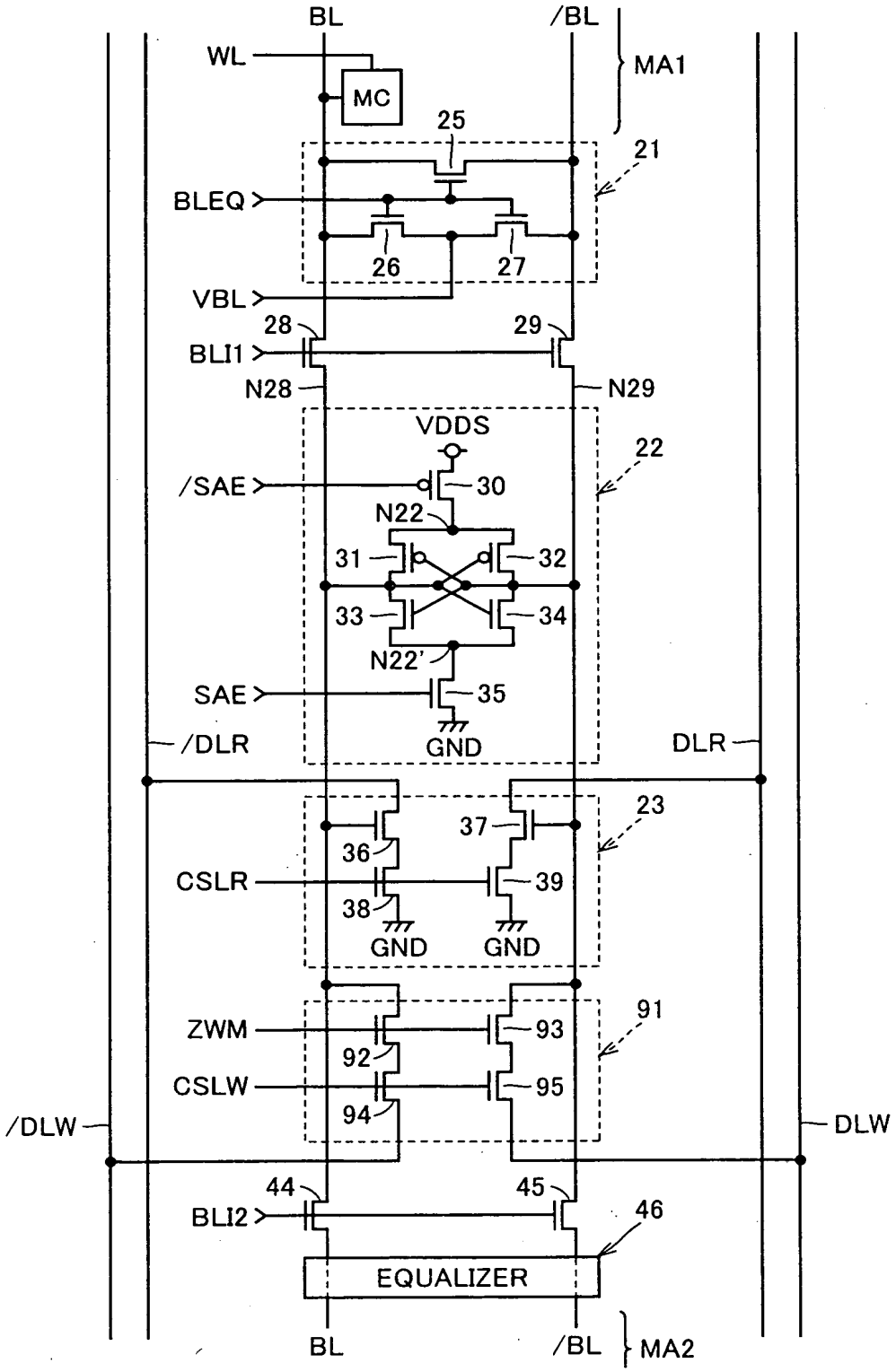

BL
/BL
WL
MC
MA1
25
21
BLEQ
26
27
VBL
28
29
BLI1
N28
N29
VDDS
22
/SAE
30
N22
31
32
33
34
N22'
SAE
35
GND
/DLR
DLR
23
37
36
CSLR
39
38
GND
GND
91
ZWM
93
92
CSLW
95
94
/DLW
DLW
44
45
BLI2
46
EQUALIZER
BL
/BL
MA2

FIG.10

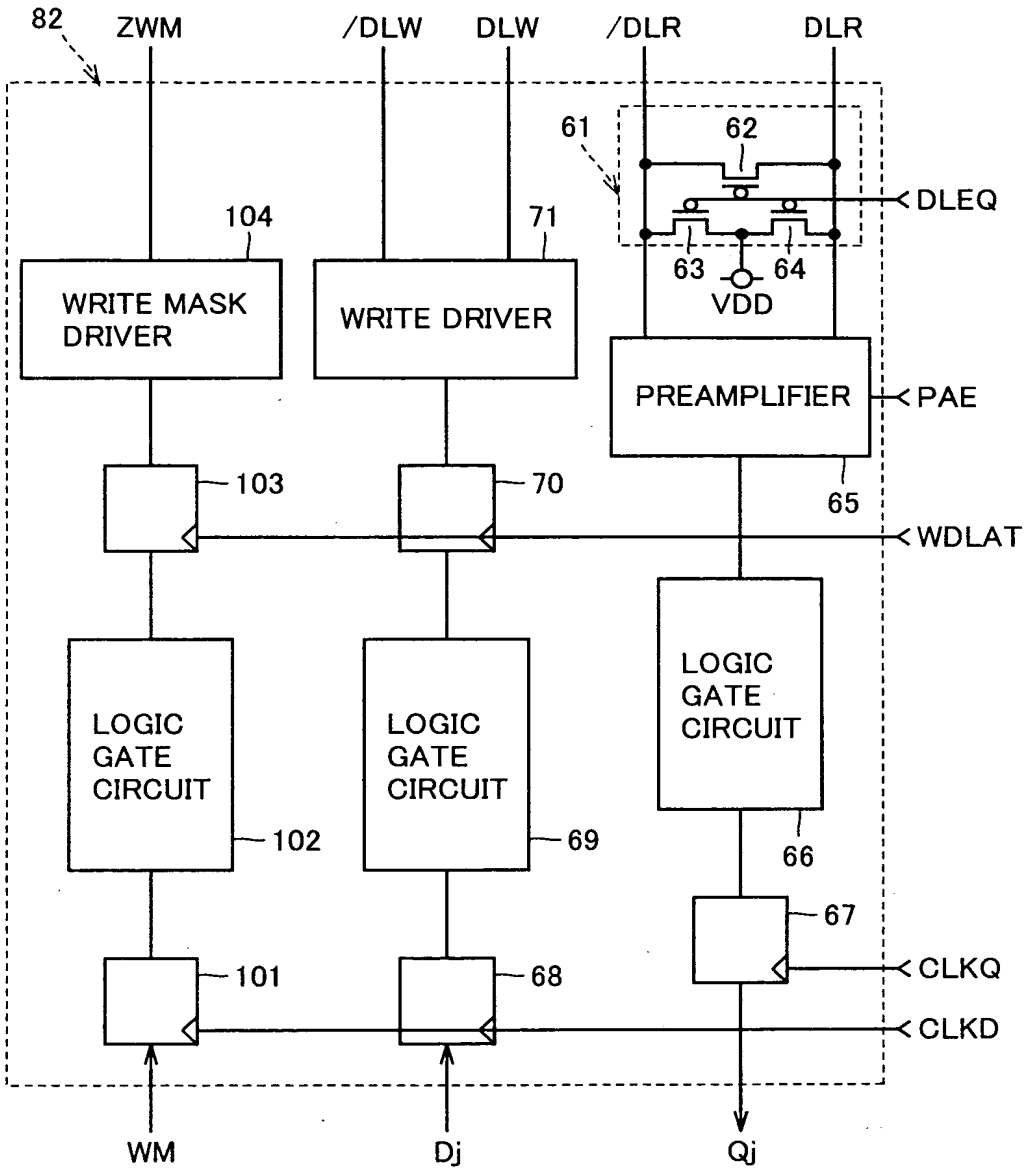

82
ZWM
/DLW
DLW
/DLR
DLR
61
62
DLEQ
104
71
63
64
VDD
WRITE MASK DRIVER
WRITE DRIVER
PREAMPLIFIER
PAE
103
70
65
WDLAT
LOGIC GATE CIRCUIT
LOGIC GATE CIRCUIT
LOGIC GATE CIRCUIT
102
69
66
67
CLKQ
101
68
CLKD
WM
Dj
Qj

FIG.11

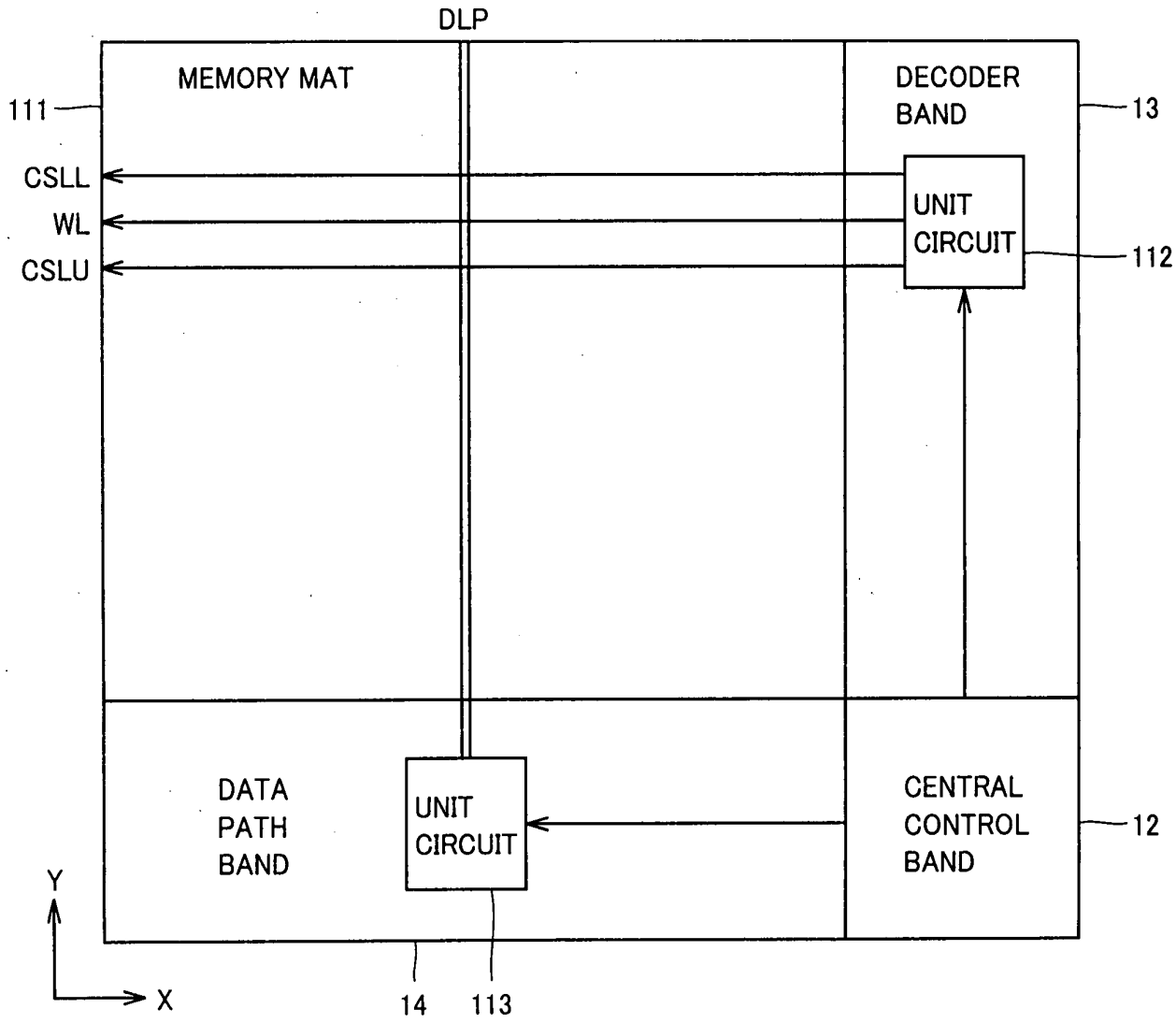

DLP
MEMORY MAT
111
DECODER BAND
13
CSLL
WL
CSLU
UNIT CIRCUIT
112
DATA PATH BAND
UNIT CIRCUIT
CENTRAL CONTROL BAND
12
Y
X
14
113

FIG.12

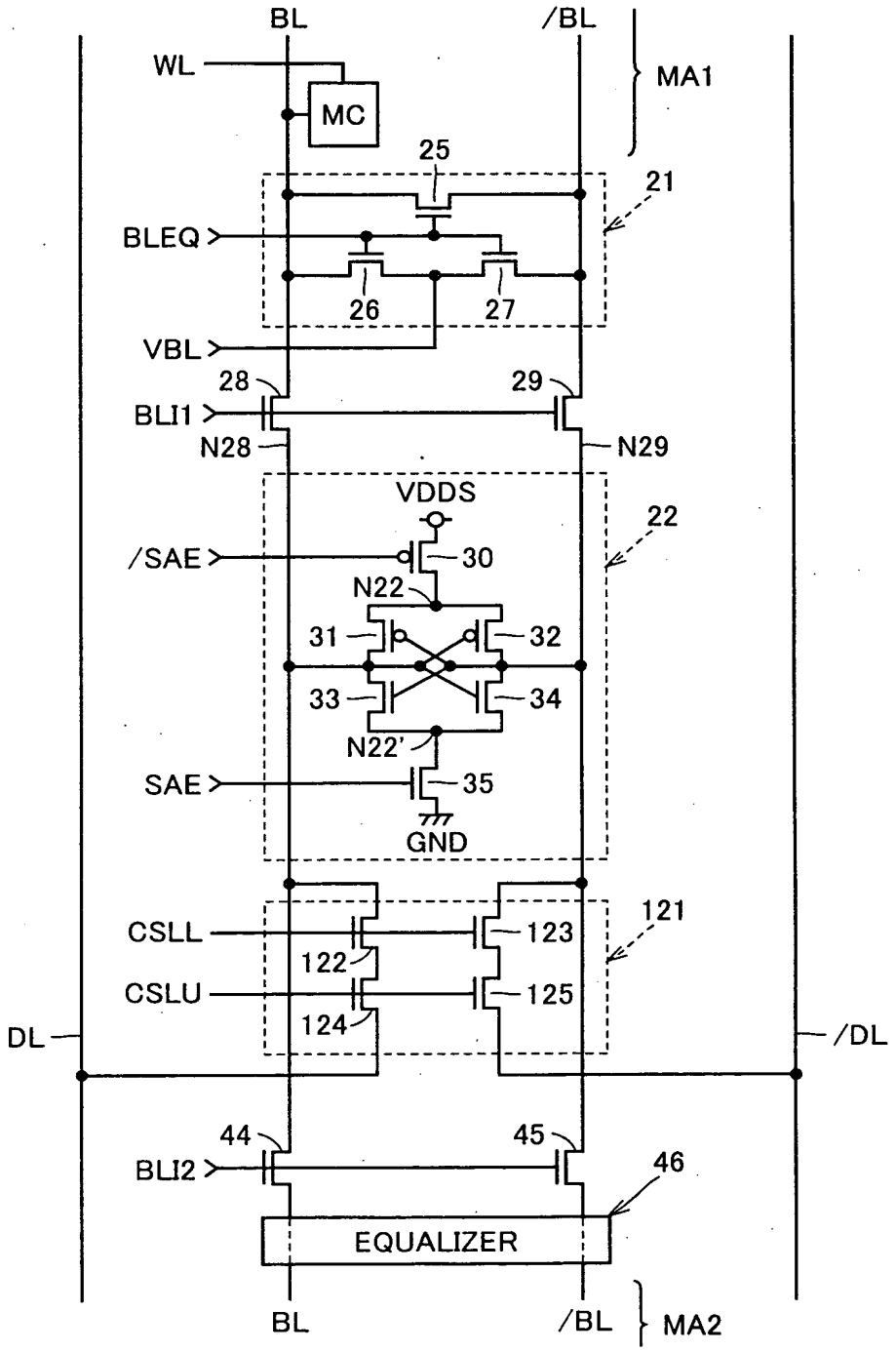

BL
/BL
WL
MC
MA1
25
21
BLEQ
26
27
VBL
28
29
BLI1
N28
N29
VDDS
22
/SAE
30
N22
31
32
33
34
N22'
SAE
35
GND
121
CSLL
123
122
CSLU
125
124
DL
/DL
44
45
BLI2
46
EQUALIZER
BL
/BL
MA2

FIG.13

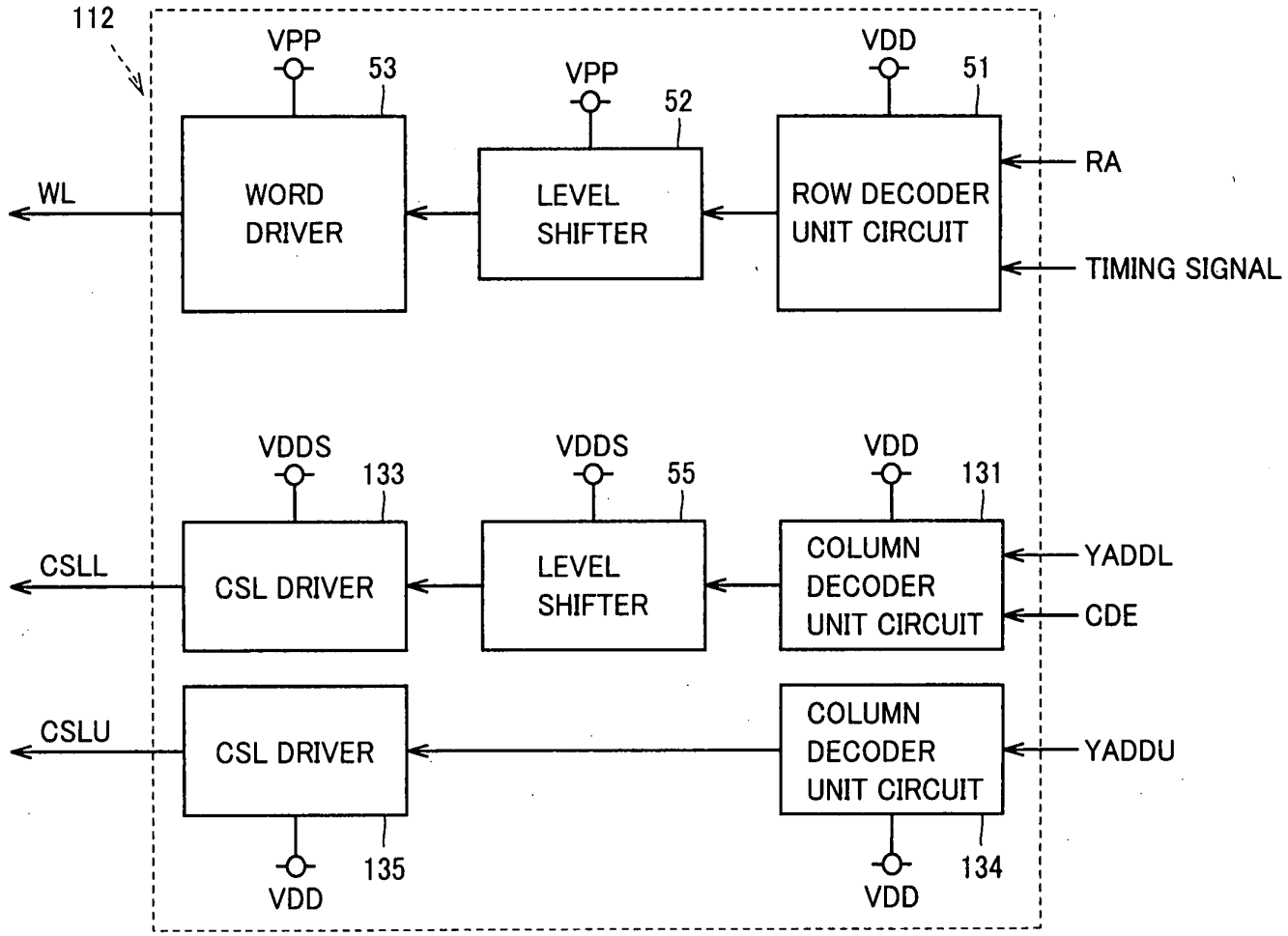

112
VPP
53
VPP
52
VDD
51
WL
WORD DRIVER
LEVEL SHIFTER
ROW DECODER UNIT CIRCUIT
RA
TIMING SIGNAL
VDDS
133
VDDS
55
VDD
131
CSLL
CSL DRIVER
LEVEL SHIFTER
COLUMN DECODER UNIT CIRCUIT
YADDL
CDE
CSLU
CSL DRIVER
COLUMN DECODER UNIT CIRCUIT
YADDU
VDD
135
VDD
134

FIG.14

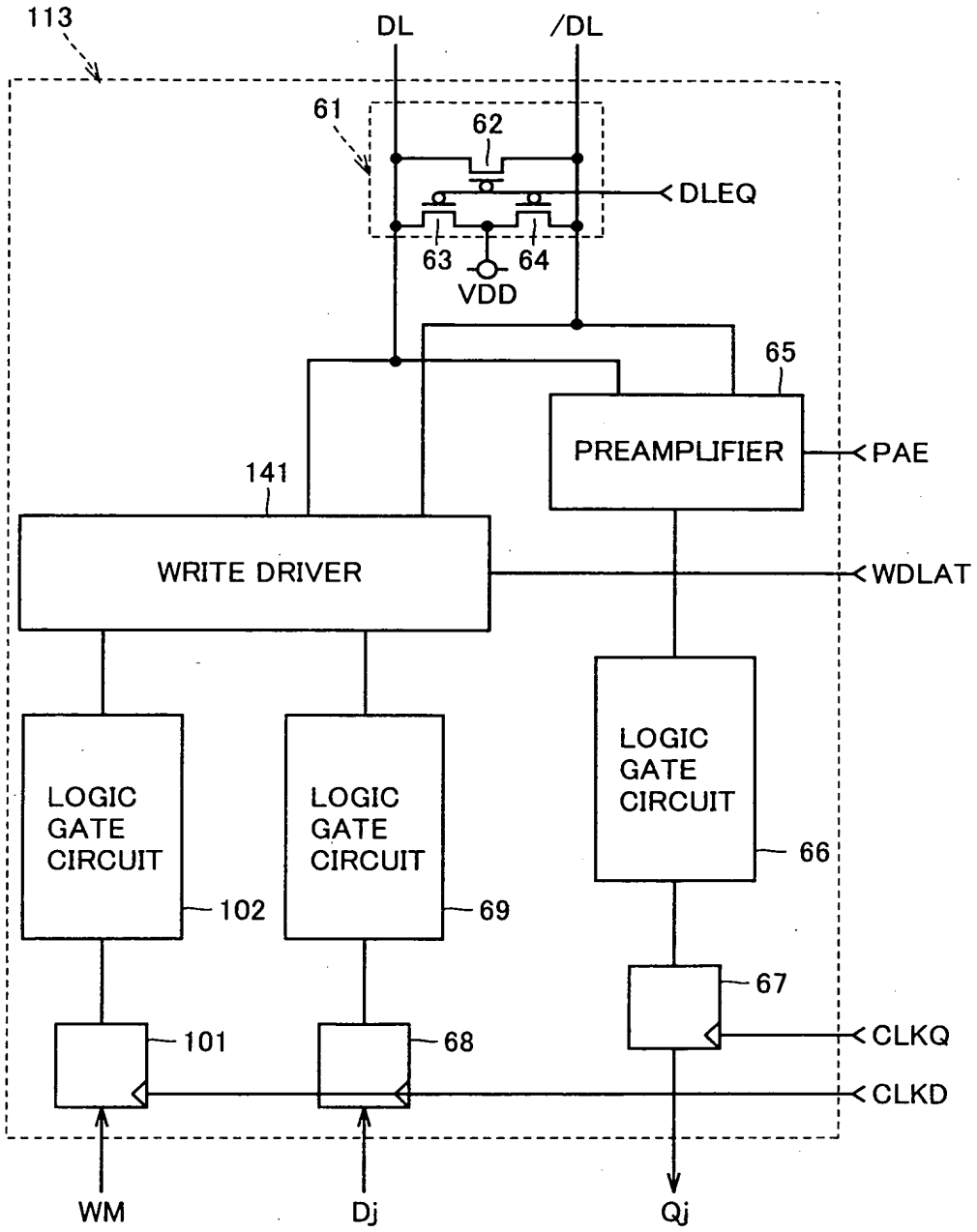
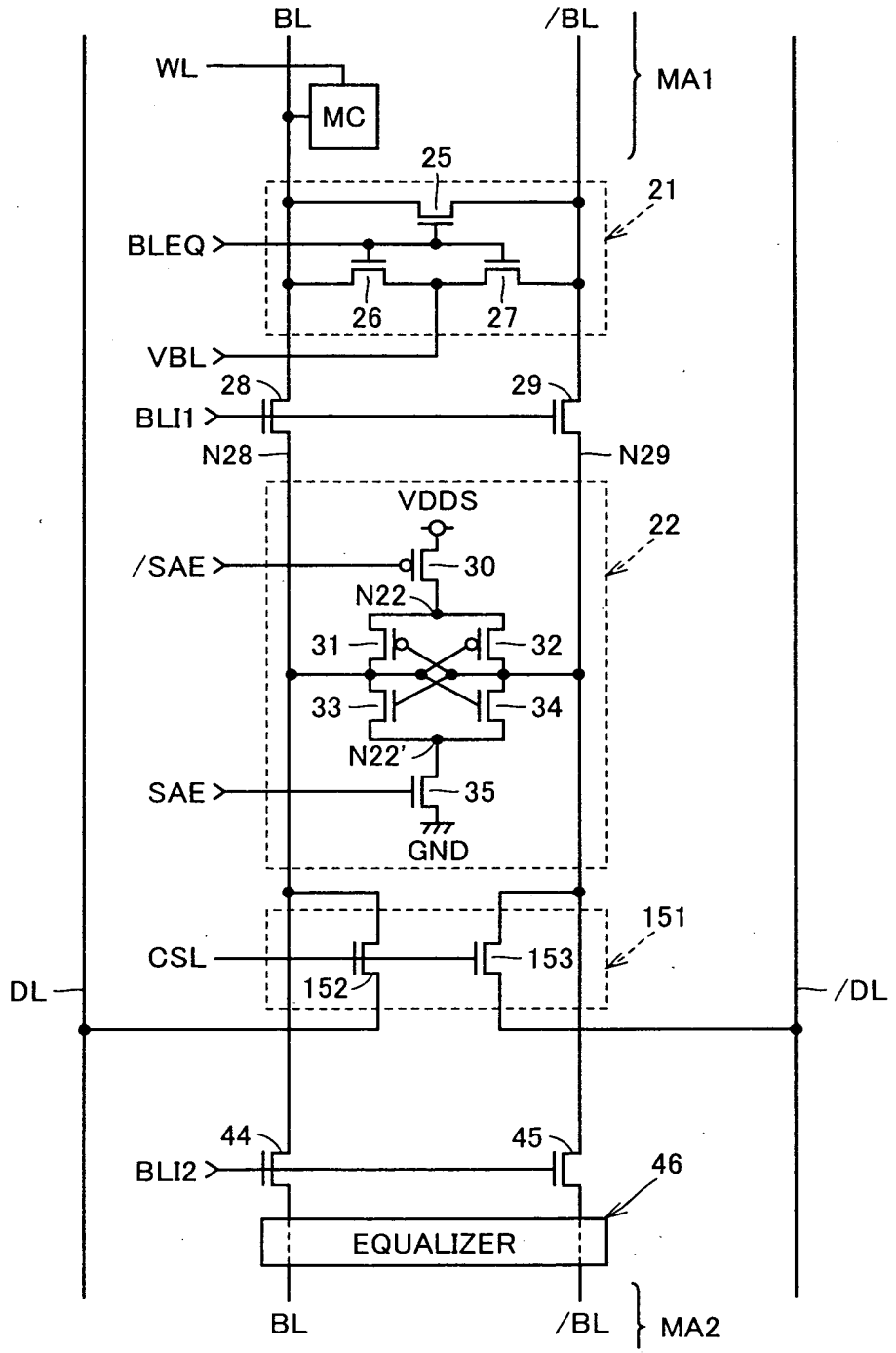

113
DL
/DL
61
62
DLEQ
63
64
VDD
65
PREAMPLIFIER
PAE
141
WRITE DRIVER
WDLAT
LOGIC GATE CIRCUIT
102
LOGIC GATE CIRCUIT
69
LOGIC GATE CIRCUIT
66
67
101
68
CLKQ
CLKD
WM
Dj
Qj

FIG.15


BL
/BL
WL
MC
MA1
25
21
BLEQ
26
27
VBL
28
29
BLI1
N28
N29
VDDS
22
/SAE
30
N22
31
32
33
34
N22'
SAE
35
GND
151
CSL
153
152
DL
/DL
44
45
BLI2
46
EQUALIZER
BL
/BL
MA2